IN THE CLAIMS

1. (currently amended): A semiconductor device comprising:

a semiconductor chip having a first main surface on which a plurality of electrode pads are provided, a second main surface which opposes said first main surface, and a plurality of side surfaces between said first main surface and said second main surface;

an extension portion which has a first surface and a second surface opposing said first surface, and which is formed in contact with said side surfaces of said semiconductor chip to surround said semiconductor chip and such that said first surface is at a substantially equal level to the level of said first main surface;

an insulating film which is formed on said first surface and said first main surface such that a part of each of said plurality of electrode pads is exposed;

a plurality of wiring patterns electrically connected to each of said electrode pads, respectively and extended from said electrode pads to the upper side of the first surface of said extension portion;

a sealing portion which is formed on said wiring patterns and said insulating film such that a part of each of said wiring patterns is exposed; and

a plurality of external terminals provided over said wiring patterns in a region including the upper side of said extension portion; and

wherein a portions of said wiring patterns on a boundary and vicinity thereof between said semiconductor chip and the extension portion are formed wider or more thickly than other portions of said wiring patterns.

2. (original): The semiconductor device according to claim 1, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals,

wherein said sealing portion is formed such that the top surface of said electrode posts is exposed.

3. (original): The semiconductor device according to claim 1, further comprising a lower base for supporting the second surface of said extension portion and the second main surface of said semiconductor chip.

4. (original): The semiconductor chip according to claim 1, wherein said electrode posts are formed from a conductive material.

5. (original): The semiconductor device according to claim 1, wherein a thin oxidation layer is formed on a surface of said electrode posts.

6. (canceled)

7. (original): The semiconductor device according to claim 1, wherein said extension portion is formed from a material having greater molding shrinkage than the molding shrinkage of said sealing portion.

8. (original): The semiconductor device according to claim 4, wherein said extension portion is formed from a liquid resin having a coefficient of linear expansion, within a lower temperature range than a glass transition temperature, of less than 1.5×10^{-5}/ °C and a modulus of elasticity within a range of 7.8 to 22 GPa.

9. (original): The semiconductor chip according to claim 1, wherein the external terminals are formed as solder balls.

10. (original): The semiconductor chip according to claim 1, wherein the external terminals are formed as lands.

11. (new): A semiconductor device comprising:

a semiconductor chip having a first main surface on which a plurality of electrode pads are provided, a second main surface which opposes said first main surface, and a plurality of side surfaces between said first main surface and said second main surface;

an extension portion which has a first surface and a second surface opposing said first surface, and which is formed in contact with said side surfaces of said semiconductor chip to surround said semiconductor chip and such that said first surface is at a substantially equal level to the level of said first main surface;

an insulating film which is formed on said first surface and said first main surface such that a part of each of said plurality of electrode pads is exposed;

a plurality of wiring patterns electrically connected to each of said electrode pads, respectively and extended from said electrode pads to the upper side of the first surface of said extension portion;

a sealing portion which is formed on said wiring patterns and said insulating film such that a part of each of said wiring patterns is exposed; and

a plurality of external terminals provided over said wiring patterns in a region including the upper side of said extension portion;

wherein a thin oxidation layer is formed on a surface of said electrode posts.

12. (new): The semiconductor device according to claim 11, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals,

wherein said sealing portion is formed such that the top surface of said electrode posts is exposed.

13. (new): The semiconductor device according to claim 11, further comprising a lower base for supporting the second surface of said extension portion and the second main surface of said semiconductor chip.

14. (new): The semiconductor chip according to claim 11, wherein said electrode posts are formed from a conductive material.

15. (new): The semiconductor device according to claim 11, wherein said extension portion is formed from a material having greater molding shrinkage than the molding shrinkage of said sealing portion.

16. (new): The semiconductor device according to claim 15, wherein said extension portion is formed from a liquid resin having a coefficient of linear expansion, within a lower temperature range than a glass transition temperature, of less than 1.5×10^{-5} / °C and a modulus of elasticity within a range of 7.8 to 22 GPa.

17. (new): The semiconductor chip according to claim 11, wherein the external terminals are formed as solder balls.

18. (new): The semiconductor chip according to claim 11, wherein the external terminals are formed as lands.